Listing of the Claims: (This listing of the claims will replace all prior versions, and listings, of claims in the application. No amendments to the claims have been made.)

Claims 1 – 21 (cancelled)

22. (previously presented) A circuit for use with a multi-port memory device having an array of memory cells serviced by row decoders and column decoders, comprising;

an input/output control circuit for writing data into and reading data out of the array;

a plurality of storage devices for storing information; and

a control circuit for identifying which of a first and a second system may have access to the array, for controlling the operation of said plurality of storage devices and said input/output control circuit, and for defining the privileges which the first and second system have with respect to the array of memory cells in response to mode control signals, said mode control signals for simultaneously defining read and write access privileges for both of said first and second systems.

23. (original) The circuit of claim 22 wherein said plurality of storage devices store information from the system not having access to the array for a period of time sufficient to enable the system having access to the array to complete an operation.

24. (original) The circuit of claim 22 wherein said control circuit includes an arbitration circuit having a first circuit for determining a valid access to said array by one of the systems, a second circuit for detecting when an access is completed, and a third circuit responsive to said first circuit and said second circuit for generating a busy signal.

25. (original) The circuit of claim 24 wherein said third circuit generates said busy signal when a valid access to said array is determined and ceases generation of said busy signal when an end of cycle is detected for the system having access to said array.

26. (original) The circuit of claim 22 wherein the array of memory cells is divided into two sections, and wherein said mode control signals determine if both systems have read/write privileges to both said sections, if one system has read/write privileges to both said sections while said other system has read/write privileges to only one section of said array.

and if one system has read/write privileges to one section of said array while the other system has read/write privileges to the other section of said array.

27. (original) The circuit of claim 26 wherein said control circuit includes a mode circuit having a comparator circuit for determining the section specified in an address, a decoder circuit for decoding said mode control signals, and a logic circuit responsive to said comparator circuit and said decoder circuit for producing read and write control signals.

28. (previously presented) A circuit for transferring data between at least two ports and a single memory array, comprising:

an input/output control circuit for transferring data between the ports and the memory array;

a first storage device positioned between said input/output control circuit and the ports;

first and second row decoders, each responsive to addresses corresponding to data at one of the ports, for addressing a row within the array;

first and second column decoders, each responsive to addresses corresponding to data at one of the ports, for addressing a column within the array;

a second storage device for storing addresses to be input to said first and second row decoders and said first and second column decoders; and

a control circuit for producing signals for controlling the operation of said input/output control circuit and said first and second storage devices and for defining the privileges which the ports have with respect to the array of memory cells in response to mode control signals, said mode control signals for simultaneously defining read and write access privileges for both of said first and second ports.

29. (original) The circuit of claim 28 wherein the first and second storage devices store information from the port not having access to the array for a period of time sufficient to enable the port having access to the array to complete an operation.

30. (original) The circuit of claim 28 wherein said control circuit includes an arbitration circuit having a first circuit for determining a valid access to said array by one of the ports, a second circuit for detecting when an access is completed, and a third circuit responsive to said first circuit and said second circuit for generating a busy signal.

31. (original) The circuit of claim 30 wherein said third circuit generates said busy signal when a valid access to said array is determined and ceases generation of said busy signal when an end of cycle is detected for the port having access to said array.

32. (original) The circuit of claim 28 wherein the array of memory cells is divided into two sections, and wherein said mode control signals determine if both ports have read/write privileges to both said sections, if one port has read/write privileges to both said sections while said other port has read/write privileges to only one section of said array, and if one port has read/write privileges to one section of said array while the other port has read/write privileges to the other section of said array.

33. (original) The circuit of claim 32 wherein said control circuit includes a mode circuit having a comparator circuit for determining the section specified in an address, a decoder circuit for decoding said mode control signals, and a logic circuit responsive to said comparator circuit and said decoder circuit for producing read and write control signals.

34. (previously presented) A multi-port memory device responsive to first and second systems, comprising:

an array of memory cells;

a first input/output port responsive to the first system and a second input/output port responsive to the second system;

an input/output control circuit responsive to said first and second input/output ports, said input/output control circuit for writing data into and reading data out of said array;

first decoders responsive to the first system, said first decoders for producing first signals for accessing a cell within said array;

second decoders responsive to the second system, said second decoders for producing second signals for accessing a cell within said array;

a plurality of storage devices; and

a control circuit responsive to the first and second systems for identifying which of the systems is entitled to access to said array, for controlling the operation of said input/output control circuit and said plurality of storage devices and for defining the privileges which the first and second system have with respect to the array of memory cells in response to mode control signals, said mode control signals for simultaneously defining read and write access privileges for both of said first and second systems.

35. (original) The memory device of claim 34 wherein the plurality of storage devices store information fr m the system not having access to the array for a period of time sufficient to enable the system having access to the array to complete an operation.

36. (original) The memory device of claim 34 wherein said control circuit includes an arbitration circuit having a first circuit for determining a valid access to said array by one of the systems, a second circuit for detecting when an access is completed, and a third circuit responsive to said first circuit and said second circuit for generating a busy signal.

37. (original) The memory device of claim 36 wherein said third circuit generates said busy signal when a valid access to said array is determined and ceases generation of said busy signal when an end of cycle is detected for the system having access to said array.

38. (original) The memory device of claim 34 wherein said array of memory cells is divided into two sections, and wherein said mode control signals determine if both systems have read/write privileges to both said sections, if one system has read/write privileges to both said sections while said other system has read/write privileges to only one section of said array, and if one system has read/write privileges to one section of said array while the other system has read/write privileges to the other section of said array.

39. (original) The memory device of claim 38 wherein said control circuit includes a mode circuit having a comparator circuit for determining the section specified in an address, a decoder circuit for decoding said mode control signals, and a logic circuit responsive to said comparator circuit and said decoder circuit for producing read and write control signals.

40. (previously presented) A multi-port memory device responsive to first and second systems, comprising:

an array of memory cells;

a first input/output port responsive to the first system and a second input/output port responsive to the second system;

means, responsive to said first and second input/output ports, for writing data into and reading data out of said array;

first means, responsive to the first system, for producing first signals for accessing a cell within said array;

second means, responsive to the second system, for producing second signals for accessing a cell within said array;

means for storing; and

third means responsive to the first and second systems for identifying which of the systems is entitled to access to said array, for controlling the operation of said means for reading and writing and said means for storing and for defining the degree of access which the two systems have to the array in response to mode control signals, said mode control signals for simultaneously defining read and write access privileges for both of said first and second systems.

41. (original) The memory device of claim 40 wherein said means for storing stores information from the system not having access to the array for a period of time sufficient to enable the system having access to the array to complete an operation.

42. (original) The memory device of claim 40 wherein said third means includes an arbitration circuit having a first circuit for determining a valid access to said array by one of the systems, a second circuit for detecting when an access is completed, and a third circuit responsive to said first circuit and said second circuit for generating a busy signal.

43. (original) The memory device of claim 42 wherein said third circuit generates said busy signal when a valid access to said array is determined and ceases generation of said busy signal when an end of cycle is detected for the system having access to said array.

44. (original) The memory device of claim 40 wherein said array of memory cells is divided into two sections, and wherein said mode control signals determine if both systems have read/write privileges to both said sections, if one system has read/write privileges to both said sections while said other system has read/write privileges to only one section of said array, and if one system has read/write privileges to one section of said array while the other system has read/write privileges to the other section of said array.

45. (original) The memory device of claim 44 wherein said third means includes a mode circuit having a comparator circuit for determining the section specified in an address, a

decoder circuit for decoding said mode contr l signals, and a logic circuit responsive to said comparator circuit and said decoder circuit for producing read and write control signal.

46. (previously presented) A method of operating a multi-port memory device of the type having an array of memory cells each represented by a unique row and column address, said multi-port memory device being responsive to two systems, said method comprising:

producing first signals for identifying an address of a cell within said array to which access is sought by the first system;

producing second signals for identifying an address of a cell within said array to which access is sought by the second system;

identifying which of the systems is entitled to access to said array in response to mode control signals, said mode control signals for simultaneously defining read and write access privileges for both of said first and second systems, and producing the signals to enable said access; and

storing information from the system not granted access.

47. (original) The method of claim 46 wherein the information is stored for a period of time sufficient to enable the system having access to complete an operation.

48. (original) The method of claim 47 additionally comprising the step of performing an operation corresponding to the stored information after said period of time has elapsed.

49. (original) The method of claim 46 additionally comprising the steps of determining a valid access to an address in said array by one of the systems, detecting when an access is completed, and generating a busy signal in response to said determining and detecting steps.

50. (original) The method of claim 49 wherein said busy signal is generated when a valid access to an address is determined and ceases to be generated when an end of cycle is detected for the system having access to said address.

51. (original) The method of claim 46 wherein said array of memory cells is divided into two sections, and wherein said identifying step includes the steps of determining if both systems have read/write privileges to both said sections, if one system has read/write privileges to both said sections while said other system has read/write privileges to only one

section of said array, and if one system has read/write privileges to one section of said array while the other system has read/write privileges to the other section of said array.

52. (original) The method of claim 51 wherein said identifying step includes the steps of determining the section specified in an address, decoding said mode control signals, and producing read and write control signals in response to said determining and decoding steps.

53. (original) The method of claim 46 additionally comprising the step of arbitrating between which of the systems may have access to the array.